Project profile

CT208 | Research on optimal architecture and integration of 22/20 nm node core digital CMOS technology – electrical proof of concept [REACHING 22]

The REACHING 22 project is researching the optimal transistor architecture and its integration for 22/20 nm node core CMOS technology. This CATRENE project intends to provide an electrical proof of concept. It is particularly active in fully-depleted silicon-on-insulator (FDSOI) process technology with the development of an appropriate engineered substrate. An electrical benchmark will be made between bulk silicon and FDSOI architectures based on transistor performance and on a design library evaluation mask set. REACHING22 is part of a series of more Moore projects led by STMicroelectronics that constitute a coherent strategic development of successive digital CMOS technologies.

Although bulk CMOS technologies are reaching some intrinsic limits when gate lengths are drawn below 25 nm, the major issue is the need to scale geometries further whilst keeping acceptable dynamic and static power on one hand and device variability at ever lower operating voltages on the other. This has caused some observers of the global semiconductor industry to foresee lower productivity gain as transistors keep shrinking.

Most of the integrated device manufacturers in the field of logic CMOS have gone 'fablite' for their leading edge products – that is they are no longer producing devices themselves but relying on foundries. IBM leads the ISDA alliance on leading-edge technology development in which STMicroelectronics is a partner.

Intel – the digital technology leader for microprocessors – is also becoming a player in the low power embedded microprocessor area. It has announced its choice of transistor architecture at 22 nm based on a fully-depleted 3D FinFET double-gate transistor architecture built directly on bulk silicon.

The CATRENE CT208 REACHING 22 project has therefore launched perfectly on time to decide whether or not fully-depleted devices are mandatory at 22 nm and what benefits they offer in low-power applications.

Cost/performance squeeze

For the first time, at the 22 nm node, no decrease is expected in the cost of a function by shrinking from one node to the next. Technology complexity, mask costs and design variability could offset the performance gain by the transistor area reduction and the speed boost coming with it.

If the price of wafer processing increases by 40% when moving to the 22 nm node, the cost per gate would not decrease at that node. However at 22 nm, traditional planar bulk CMOS architecture is so well known and entrenched that it must be still studied before it can be ruled out.

Fully-depleted silicon-on-insulator (SOI) technologies have the potential to address the cost/performance squeeze facing the future 22 nm node as long as substrate materials are available in adequate volume, quality and price. REACHING 22 is therefore focusing on both bulk and SOI technologies at the 22/20 nm level. While multiple transistor architectures are possible on thin film, this project will focus primarily on planar fully-depleted SOI (FDSOI) architecture.

FDSOI provides a low risk option for semiconductor companies seeking to take advantage of the benefits of fully-depleted transistor architecture while leveraging existing design and manufacturing capabilities. SOI substrates increase the overall

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	✔
Digital lifestyle	
Design technology	✔
Sensors and actuators	
Process development	✔
Manufacturing science	✔
More than Moore	
More Moore	✔
Technology	22/20 nm

PROCESS DEVELOPMENT

Partners:
CEA-LETI
IMEP/INPG
LTM/CNRS
SOITEC
ST-Ericsson
STMicroelectronics
Université Catholique de Louvain (UCL)

Project leader:
Gilles Thomas
STMicroelectronics

Key project dates:
Start: April 2011
End: March 2014

Countries involved:
Belgium
France

product cost but the implementation of fully-depleted transistors can solve scaling, leakages and variability issues associated with shrinking. Globally, the resulting CMOS technology is less complex and therefore enjoys better manufacturability and yield.

The ambition of REACHING 22 is to cover the first phase of the 22/20 nm technology deployment, although the test mask set will go well beyond the simple proof of concept traditionally based on an elementary SRAM cell.

Competitive beyond 28 nm

The multifunctional system-on-chip (SoC) devices needed at the heart of the next generation of high performance but low power wireless multimedia processors exhibit different requirements from mono-functional processors in the main. REACHING 22 supports the existing roadmap of one European semiconductor manufacturer aimed at maintaining a vibrant ecosystem in More Moore technology. This CATRENE project maintains a European chipmaker in a position in to develop strategic state-of-the-art digital electronics. In particular, the company is keen to focus on low power semiconductor technologies to conserve energy and extend battery life in handheld devices.

Constant miniaturisation has led to a power crisis causing excessive heat generation in silicon chips. To achieve an overall power-optimised system, several measures have to be developed, including:

- New semiconductor process options to reduce dynamic and static power;
- New device architectures; and
- New circuitries with a standby option and partial system shut-off to reduce power consumption.

REACHING 22 will provide accurate analytical and technology computer-aided design models to help the development, assessment and optimisation of the different technology options. Several test structures will be implemented on silicon to assess FDSOI technology for SoC and ultra low-power applications.

International collaboration

Even if core CMOS technology tends to align with a limited number of internationally accepted standards, some companies want to pursue the possibility of distinguishing themselves by having a larger range of proprietary technologies. This enables the creation of added value.

Such an initiative within CATRENE helps maintain a group of academic and professional research institutes in Europe capable of keeping up with the developments of leading-edge semiconductor technologies.

Basic process modules will be developed, targeting compatibility with both the SOI and the bulk approaches. The main activity will be carried out in the 300 mm wafer fabrication site of Crolles in France with international collaboration.

Key enabling technology

22 nm node technologies, modules and the first screening of possible options are being actively investigated by the major global research and development alliances with the ultimate goal of introducing them to industrial production in 2014 or 2015 at the latest.

Through this strategic CATRENE project, the actors involved have the possibility of satisfying the challenges of worldwide business requirements and consolidating their leadership in a key enabling technology – instrumental to the communications sector. Innovation has never been more important, so a continuous and sustained effort is of paramount significance for the health of this sector in Europe.

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CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.